SOC Design Issues: A Review

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Abstract: **Over the years as the complexity and cost of Integrated Circuits increased and at the same geometry decreased at an exponential rate, the IC industry began to use a new design methodology, System on Chip (SOC) Design. SOC is basically an integrated circuit that contains all the components of a system on a single chip. They are fabricated using various types of cores. Due the use of these different types of cores coupled with the increasing complexity of integration, interfacing and other verification tests at different levels of integration, various design issues arise. This paper presents a study of the design issues encountered during SOC design.**

Key words: **SOC, cores, IP**

I. INTRODUCTION

The semiconductor industry has continued to make impressive improvements in the achievable density of very large-scale integrated (VLSI) circuits [1]. In order to keep pace with the levels of integration available, design engineers have developed new methodologies and techniques to manage the increased complexity inherent in these large chips. One such emerging methodology is system-on-chip (SoC) design. For an SOC to provide full functionality for an application on an IC, it is designed by stitching together different multiple stand alone VLSI designs. They can be designed either by using; ASIC vendor design where all the components are manufactured by a single vendor; or integrated design where some components are manufactured by the vendor and others are obtained from other source; or by a desktop design where all the components are stitched together from other sources by a fables company[2,8]. These design strategies are valid and very effective for SOC design.

With greater device integration, system design becomes more complex and challenging. Though the size is decreasing, important design factors such as power consumption, LVS (Layout vs Schematic), DRC (Design Rules Check), timing issues, design validation etc have to be kept in mind. These parameters need to be optimized for the new design technologies. Due to this mismatch several design issue arise. These issues include power efficiency, design for test, latency. One possible solution is design re-use. The exis ting cores or IP (Intellectual Property) can be reused to save time and resources and also to meet the demand in a timely manner. New SOC's are built from circuit blocks from design of previous ones. These reusable IP cores may include embedded processors, memory blocks, interface blocks, analog blocks, and components that handle application specific processing functions[3,4].

II. DESIGN ISSUES

Power Consumption

It is difficult to provide power to the increasing number of integrated transistors on a single chip. Hence, the system should have high performance and low power consumption. This emphasizes the need for low power designs as power consumption is a key parameter. Because the power dissipation per transistor is not falling at the rate that gate density is increasing, the power density of future SoCs is set to increase. Thus, we must reduce overall system power consumption by using system architecture design rather than relying on process technology alone[5].

Latency

This increasing gap between processor and memory speeds is a well-known problem, named the memory wall.[4] For this problem, the designers are integrating embedded memories into the same chip. Also, due the increasing number of components, it becomes very difficult to provide simultaneously same clock signals to every component. This becomes a major design issue as we proceed further to timing analysis and verification for the SOC.

Design for Verification

Design for verification and for testing is one the most time consuming step in chip design flow. Even a minor change in the circuit prompts the designer to re-evaluate the performance of the device and re-verify the timing analysis of the circuit. As a billion components are integrated onto a single chip, design validation becomes more time consuming. Co-development method i.e. using both hardware and software design helps in reducing the time spent on verification and testing. Moreover, while designing SOC's, it happens that different IP are taken from different vendors and stitched together on a single. Hence a need arises to come up with a generalized effective design strategy for SOC.

Reconfigurable Logic

Designers have used field-programmable gate arrays (FPGA) in board-level designs for a long while. To create high performance, versatile platforms, some architectures start incorporating logic operations and interconnects that can be reconfigured during run time. Adding reconfigurable logic to the SOC provides flexibility for changing functionality after fabrication. Compared to programmable processors, these architectures offer the potential to achieve higher performance and power efficiency with greater flexibility.

Static Timing Analysis

With multiple voltage, libraries may not be characterized at the exact voltage we are using, timing analysis becomes much more complex. The end result is that the design should meet timing and power requirements for all the mode/corner scenarios. Designers must ensure that the correct level shifters, retention cells, and other design elements have been accurately placed for each of the different power domains, also verify bulk and well connections at the transistor level. There are tools from EDA companies help automate these checks[6].

Other Design Issues

As mentioned earlier, designers are now using embedded memories which are integrated on the same chip as it is easier to synchronous the memories with the system and eliminates the need for extra hardware. Challenges arise when trying to balance efficiency and power. SRAM provides high performance, while flash memory is the best solution in terms of power consumption.[4] Similarly there are multiple processors also integrated on the same chip and we can use parallel pipelining to increase the efficiency of the SOC.

When using portability methodology certain other design issues arise. For example, layout dependent step sizes, aspect ratio misfits and non-netlisted core. Timing issues include clock redistribution; Hard core width and spacing disparities; Antenna rules disparities; RC parasitic due to chip layers; Timing reverification; Circuit timing.

These issues can be solved by a range of associations that have been developed to provide guidelines for the design of cores and how to use them. Some of these associations are; Pinnacles Component Information Standards (PCIS) by Reusable Application-Specific Intellectual Property Developers (RAPID); Electronic Component Information Exchange (ECIX) program by Silicon Integration Initiative (Si2); Embedded core design and test specifications by Virtual socket Interface (VSI) Alliance.

III. CONCLUSION

As the VLSI technology moves forward, more and more functionality is added to SOC's. These SOC's have a large number of clock and power components and many IPs and memories. These types of multi-power domain SOCs are complex and present new integration challenges because many blocks have different operating modes at different voltages, different clock period and duty cycles of each block being awake, asleep or in shutdown mode. We must pay more attention to applications that dictate modes of operations, power and battery life requirements[7]. The SoC architecture must consider overall system performance, flexibility, and scalability, power/thermal management, system partition (among digital, analog, on-chip, or off-chip), architecture partition (between hardware and software), algorithm developments for emerging applications, and so on.[4] While power gating and other techniques are effective today, these techniques may not be enough for many IOT low-power SOCs. We have to think in terms of design- for- power in terms of energy consumptions at all levels of design including overall system/ application, architectural, power management, RTL, DFT, and physical implementation in addition to technology and process advancements[7].

IV. REFERENCES

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