Built in Self-Test: A REVIEW

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Abstract: **Memories take important role in development of new technology because memory may fail during their operation with their expected life time. So memory is needed to keep on test mode and validates that whether it is error free or not. In the virtue of submicron effect redundant circuit must kept on chip to replace faulty part. That method is known as BIST. Module synthesizes the cut the faulty part. The chip tastes the circuit each time before they start up. The main purpose of this to have error free circuit, small area and low power. The paper concluded some test problems and its reliable solution.**

Key words: **Built in self-test, test pattern generation, module synthesis**

I. INTRODUCTION

BIST is designed so that it allows a machine to test itself. It is a method of testing microprocessor, microcontroller. It helps to deal us with large transistors in a circuit. It helps to reduce the complexity of the circuit. The cost is reduced in two ways. Reduction on complexity of circuit of the test/ probe set up, reduction on no. of I/O signals that must be driven under test control. Test pattern generator circuit and output analyzer are placed on the circuit. In order to test microprocessor there are 3 blocks in microprocessor fetch unit, decode unit, execution unit. The fetch unit obtains the opcode of the next instruction based on the address in the program. It is decode by operation based logic which generate a function of select and control signal for the execution unit. Based on this control signal logic blocks computers its function while execution. The operand or data is obtained from the system memory for computation. The basic part of BIST is LFSR, CUT AND MSR. A large no. of test pattern is generated in these blocks and compare with error free responses. Whether the circuit is working properly or not. Testing only defines the design process not fabrication process. The data in LFSR are obtained as operand on the instruction provided by TCR. The computed result is stored in MISR.

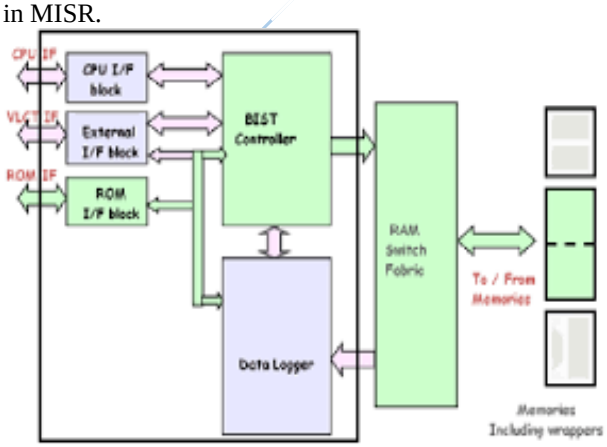

Fig1. BIST implementation with complex logic unit[1]

II. STEPS

The testing sequence is as follow;

1. Active mode: in this mode the data in TCR is accepted as instruction rather the instruction in fetch unit.
2. Initialize TCR, LSFR, and MISR either by control signal or direct control signal.
3. Load TCR with the opcode of an instruction. Based on implementation load can be either serial or parallel.
4. Clock LFSR and MISR for a fixed no. of cycle or 2^{n-1} cycles for n bit lfsr. Let us take an example if we have 2000 clocks TCR is executed 2000 times with 2000 different operands.
5. Take out the content of MISR & determine pass or fail.
6. Compare the content of MISR with precomputed logic function to determine if there is any fault. This is done by (ATE) automatic test equipment.
7. Repeat step 2 & 6 until all the instruction are exercised.

The sequence of operation assumes that after design completion, a simulation test bench is developed that exercise all instruction with LFSR data and MISR signature recorded in after each run[1]. Thus fault free MISR content after each execution is known through simulation[2].

In case any system has on chip test controller or boundary scan the control signals are passed through it tst controller or boundary scan TAP controller.

The tap controller can be generated to test control and the data from TCR is scanned and tested through it. For example RUNBIST instruction in boundary scans the control signals are passed through TAP controller. The tap controller can be generated to test control and the data from TCR is scanned and the test response can be scanned through TAP.

Different BIST that are needed using test

1. Microcode based BIST
2. Processor based BIST
3. Hardware based BIST

III. CONCLUSION

The BIST technology is economic and also gives logic test pattern. Typically the BIST controllers that are going to be generated will have test algorithms built into itself. The faults are checked in itself. We don't need an external hardware. So that the complexity is reduced and the cost reduction is also possible. By using the separate on-chip test logic, the memory test can be performed to reduce the test time[3]. &of being able to detect the faults at system operation speed is the advantage of BIST logic embedded memory. Different BIST architecture enables efficient tests of the high-performance embedded memories that are required essentially for the computer system, and it reduces the test cost[4].

IV. REFERENCES

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