Dr. S. Syed Ameer Abbas et al. International Journal of Recent Research Aspects ISSN: 2349-7688, Vol. 4, Issue 4, Dec 2017, pp. 316-322

Design and Analysis of Low Noise Amplifier using Active Inductor in ADS

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Abstract— Low Noise Amplifier(LNA) found its significant application in wireless communication systems. LNA must be designed with high gain, low noise figure, low power, small area, low cost and good input and output matching to get higher performance. In this paper LNA is designed in three stages which are common gate amplifier , common drain amplifier and active inductor to achieve higher performance. Common drain and Common gate are used for input and output matching and to lower the noise whereas active inductor is used to obtain low power consumption and to reduce chip size. The results show that the proposed LNA is able to achieve the best performance with the simulated gain of 28.974dB, lower consumption of 0.7mW and noise figure of 5dB. This modified LNA is suitable for low voltage applications mainly in wireless communication systems.

Index Terms— Active inductor, ADS, High gain, Low power, LNA.

I. INTRODUCTION

The recent development in the field of wireless technologies have raised the importance of broadband wireless access systems. To increase the system sensitivity a Low Noise Amplifier (LNA) with good performance is mandatory since it is the first stage amplifier in the receiver.

According to Frii's formula, the first stage of the receiver contributes mainly to the overall Noise Figure (NF) of the receiver. So it is important to design LNA's with minimum NF. The main function of LNA is to amplify a very low signal. The amplification must be done without adding noise to the received signal, To maintain the required signal to noise ratio at very low power level and For the sensitive receiver the higher signal levels can be received only when the amplification is provided at the first level. By using this design, the noise can be reduced and able to achieve high the gain even when the amplifier is inoculated directly into the received signal. In Figure 1, shows that the basic of RF transmitter and receiver block diagram.The function of the transmitter is to modulate and transmit the signal whereas the RF receivers receives and demodulates the signal. Nowadays, the technology has been growing up from time to time to meet the requirement in RF transmitters and receivers such as low noise, high gain, low cost, smaller size and good input and output matching. In this proposed method, a design will be created in order to fulfill these requirements.

A LNA schematic consists of three stages which are common gate amplifier, common drain amplifier and active inductor is designed which able to achieve the best performance with a simulated gain extremely, lower power consumption ,noise figure[1].Various LNA topologies are analysed in [6].

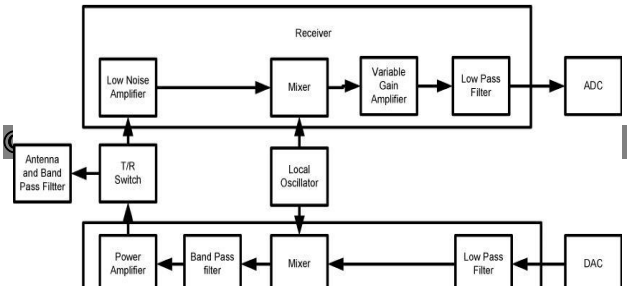


Figure 1:RF Transceiver Block Diagram

II. LNA TOPOLOGIES

Low noise amplifier is the first stage in and it is very important part in RF receivers. Hereby, low noise amplifier should be matched with the antenna characteristic. The characteristics of antenna are excellent input and output matching and high gain. To optimize the low noise amplifier design, the suitable topology should be selected for low power and low voltage.

For shunt series feedback common source topology, it is difficult to trade of among gain, small noise figure and good input and output matching with very low power consumption. For common gate topology, the gain less than 10dB with very low power consumption. Next, the noise must add to the LNA because of the resistor thermal noise for resistor termination common source topology.

Besides that, the specification is satisfied for inductive degeneration common source topology in very low power consumption but the isolation is not good enough compared to the cascade inductor source degeneration topology which can get the similar low noise amplifier performance with very low power consumption.

Lastly, for cascade inductor source degeneration topology provides higher gain with a low noise figure. Hence, there are several fundamental types of topologies for low noise

amplifier and a common low noise amplifier has been chosen for optimizing the LNA design.

III. PROPOSED METHODOLOGY

In this design there are mainly three stages in the proposed LNA. These stages are shown in Figure 2.

Figure 2: Block Diagram Of Three Stage LNA

A. Common Gate Amplifier:

Basically, common gate amplifier is widely used in electronic field and one of three basic single stages field-effect transistor (FET) topologies. The advantages by using this FET are:

i. Used as current buffer or voltage amplifier.

ii. Used as input stage for LNA

iii. Obtain input impedance matching.

The input impedance depends only on the trans-conductance of CMOS shown in equation (1) below

$$\text{:in} = \frac{1}{gm} \quad (1)$$

(iv)Potentially has lower noise.

B. Active Inductor

The active inductor has been implemented in this design which performs the same function as passive inductors. Active inductor is a combination of CMOS transistors. To design a low noise amplifier it has a fewer difficulty but it has higher flexibility to get the input and output matching, easy to design the layout and it does not have the magnetic field. For this design it does not used the real active inductor as main function but change it with transistor that perform the same function with active inductor. The advantages by using active inductor are:

i. To get lower power consumption.

ii. Used to reduce chip area

iii. Used to reduce complexity

iv. Used to reduce cost

v. Used to compensate for the affect of parasitic capacitors at high frequencies

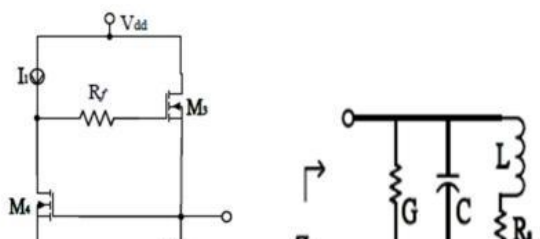


Figure 3 Active Inductor Circuit And its Equivalent Circuit

In figure 3(a) and (b), the quality factor (Q) inductance (L), and frequency (w) is calculated from the equation (2,3,4) shown below

$$\text{ } = \sqrt{\frac{gm_4 gm_3 Cgs_3 (1+R_f gds_4)}{gds_4^2 Cgs_4}} \quad (2)$$

This quality factor is high enough because it depends on Rf Feedback Resistor.

$$\text{ } = \frac{Cgs_3 (1+R_f gds_4)}{gm_4 gm_3} \quad (3)$$

v = (4)

Table 1: Specifications of LNA

After the design is implemented with the equivalent circuit, it has been improved by using double feedback with second order. Figure 4 shows the active inductor after the improvement

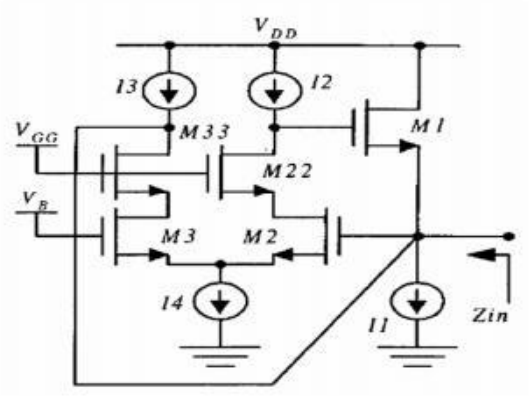


Figure 4 Double Feedback With Second Order Circuits

C. Common drain amplifier:

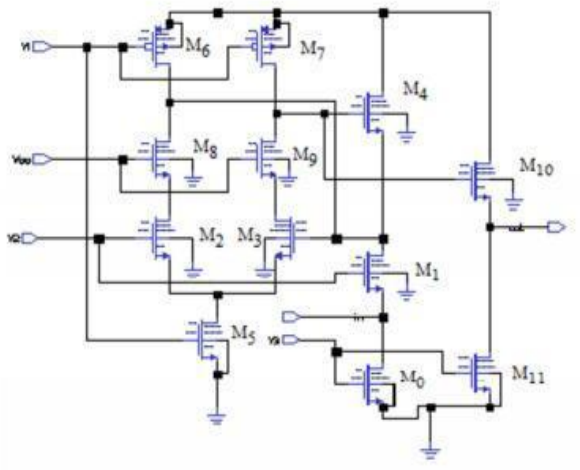
Common drain amplifier is one of three basic single-stages (FET) amplifier topologies also known as a source follower. It is usually used as a voltage buffer. The advantages by using this FET are:

i. Used as a final stage in every LNA.

ii. Capable to get small output impedance matching.

iii. Potentially has lower noise.

The proposed LNA schematic is shown in Figure 5



Transistor	Width $\frac{gm_4 gm_3}{Cgs_4 Cgs_3 (1+R_f gds_4)}$
M0	um
M1,M2,M3	2um
M4,M5	.8um
M6,M7	um
M8,M9	um
M10	.6um
M11	.7um

The design parameter of the proposed methodology is summarized in the table 1 shown above

Table 2: Transistor Width

Parameter	***pecification***
upply Voltage	*.8V*
Gain	*20dB*
Noise figure	*3dB*
ower Consumption	*50mW*
DC Current	*20mA*

The table 2 above lists the width of each transistors used in the schematic and length 0.13um for all transistor is chosen

IV. RESULTS AND DISCUSSION

Design and analysis of low noise amplifier is designed and simulated by using ADVANCED DESIGN SYSTEM(ADS) software. ADS software basics and design methods were studied in[3][4]. The DC biasing voltage values for this design are V1= 1.1, V2=0.6, V3=0.6 and Vgg=0.7 respectively.

In this design the ratios (W/L) of the transistor that used in this circuit have been fixed. The transistor length is fixed to

0.13um for all transistors while the transistor width values are different which is listed in the table 1.

A. Simulation in ADS

The Schematic is drawn in the ADS software with the components available in the software. Then perform the necessary simulation to calculate the gain, noise figure, Power dissipation.

The figure 6 shows the schematic created in ADS according to the design specification.

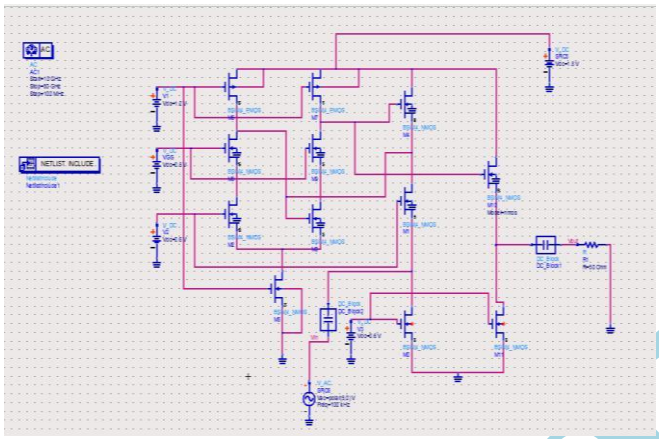


Figure 6: Schematic in ADS

In the ADS both NMOS and PMOS of BSIM4 model is chosen and the necessary netlist is inserted in the design to ensure proper working.

B. Gain Calculation

AC analysis for LNA design is obtained for the Gain calculation. To achieve the desired specifications gain, optimum transistor width, input value of DC biasing voltage was the main criteria for design of LNA. When high gain has been achieved the noise can be reduce by gain of the amplifier that captured by antenna. To obtain the gain of the LNA design, below expression(5) can be used

$$\text{Gain}=20\log_{10}\left(\frac{Vout}{Vin}\right) \qquad (5)$$

For this design the gain is successfully achieved with 28.974dB based on the design specification. Figure 7 shows the simulation result of gain in AC analysis

Figure 7: Simulation result of gain in AC analysis

C. Current and Power Measurement

For the Current Measurement the I Probe must be inserted in the design and Current can be measured. Then with the current measured average power is calculated. Figure 8 shows the schematic with I probe inserted

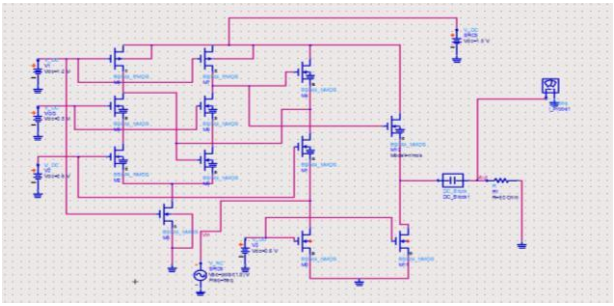


Figure 8: Schematic with I Probe

From the above simulation the current measured is 145uA and average power is around 0.7mW.

D. Parameter Analysis

The schematic is terminated with proper termination and S parameter analysis is done to obtain S_{11},S_{12},S_{21},S_{22} and Noise figure. The noise figure is found to be 5 dB. Figure 9 shows the schematic for S parameter simulation

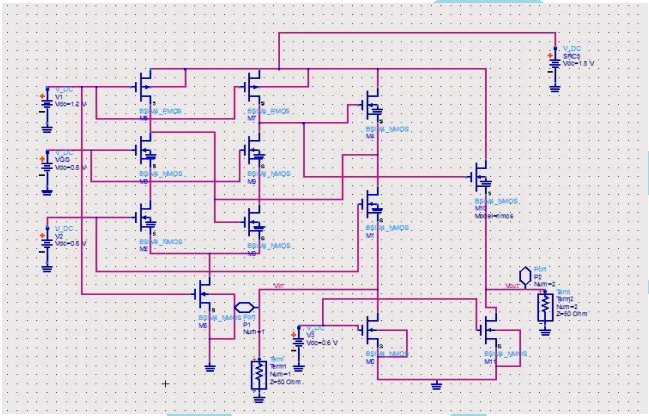


Figure 9:S parameter Analysis

The Simulation Results are summarized in the table 3 shown below

Table3: Comparison of specifications and Simulation Results

arameter	***pecification***	***imulation esult***
upply Voltage	*.8V*	*.8V*
ain	*20dB*	*8.974 dB*
oise figure	*3dB*	*dB*
ower onsumption	*50mW*	*.7mW*
C Current	*20mA*	*45uA*

V. CONCLUSION AND FUTURE WORK

An improved design of low noise amplifier using active inductor is presented in this research. The modified circuit has been design by using the ADS 0.13um CMOS technology. The objective of this design was accomplished based on the specifications of the LNA. According to the research result, the circuit is capable to achieve gain of 28.974dB, noise figure of 5dB, extremely low power consumption of 0.7mW, good input and output matching.

With the change in technology parameter ie) length of the transistors we can achieve higher performance of the LNA.And this proposed schematic can be converted in layout so that the proposed LNA can be fabricated without any off-chip components.

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